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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/814,811	03/31/2004	Philippe Messenger	A64.12-0004	5300
27367	7590	10/13/2005		
WESTMAN CHAMPLIN & KELLY, P.A. SUITE 1400 - INTERNATIONAL CENTRE 900 SECOND AVENUE SOUTH MINNEAPOLIS, MN 55402-3319			EXAMINER NGUYEN, HIEP	
			ART UNIT	PAPER NUMBER
			2816	

DATE MAILED: 10/13/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

<b>Office Action Summary</b>	<b>Application No.</b> 10/814,811	<b>Applicant(s)</b> MESSAGER, PHILIPPE	
	<b>Examiner</b> Hiep Nguyen	<b>Art Unit</b> 2816	

**-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --**

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 15 August 2005.
- 2a) ☒ This action is **FINAL**.                      2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1,3-16 and 21-23 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1,3-16 and 21-23 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 31 March 2004 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All    b) ☐ Some \* c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
  2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- |  |   |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)  | 4) <input type="checkbox"/> Interview Summary (PTO-413)<br>Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)                                   | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152)             |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)<br>Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____  |

### DETAILED ACTION

The amendment filed on 08-22-05 has been received and entered in the case. New ground of rejections necessitated by the amendment is set forth below.

#### *Claim Objections*

Claims 3, 4 and 6 are objected to because of the following informalities: claims 3, 4 and 6 depend upon cancelled claim 2. Appropriate correction is required.

#### *Claim Rejections - 35 USC § 112*

The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 1, 3-15 and 21 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Regarding claim 1, the recitation “equal to the internal reference voltage, taking into account the reference voltage” is indefinite because it is not clear as to the internal reference voltage is the same or different than the reference voltage”. Figure 4 of the present application shows only the reference voltage (3V reference).

Regarding claim 3, the recitation “the currents circulating in the connection means and in the limiting and/or detecting means are balanced” is indefinite because it is not clear what “balanced” is meant by.

Regarding claim 12, the recitation “characterized in that the power of the fourth transistor is less than that of the transistors of the second mirror, so that the latter imposes its level on the fourth transistor when it delivers the copy of the blocking current” is indefinite because it is not clear what is the “fourth transistor” in the drawing and it is not clear what the “power” is meant by. While the specification (page 6, lines 4-8) discloses that “the third transistor has the size smaller than the sizes of the transistors of the second mirror”. The same rationale is applied to claim 21.

Claims 3-15 are indefinite because of the technical deficiencies of claim 1.

***Claim Rejections - 35 USC § 102***

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1, 3-6, 8, 11, 14, 16, 22 and 23 are rejected under 35 U.S.C. 102(b) as being anticipated by Yamasaki (USP. 6,486,731).

Regarding claims 1 and 14, figure 1 of Yamasaki shows an integrated circuit means for delivering one output comprising means for generating main voltage (EX, not shown), means (RGF) for generating an internal reference (Vref). The voltage of the reference voltage (Vref) is inherently lower than the supply voltage (EX) of the circuit; means for connecting the main voltage on the output (2d) and means for detecting the voltage at the output (2b). The output voltage is equal to the reference voltage (col. 9. lines 18-23).

Regarding claims 3, 4 and 5, when the output signal is lower than the reference (Vref), the output of circuit (1) is low and the means of connecting (2d) starts to conduct until the output voltage (Vrfo) equals the reference voltage and the currents between the means of connecting (2d) and the means of detecting or limiting (2b, 2c) are balanced. The means of connecting comprises a first power transistor (2d). The connection of transistor (2d) is shown in figure 1. The reference voltage (vref) is used to supply other components of the integrated circuit (VDC).

Regarding claims 6 and 8, it is inherent that the limiting means (2b, 2c) comprises a second transistor having gate connected to the reference voltage (vref). When the predetermined voltage is reached, the circuit (2b, 2c) sends signal to “block” the first power transistor (2d).

Regarding claim 11, the gate of the first power transistor (2d) is connected to a command input (TE) via a fourth transistor (2e).

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Regarding claim 16, figure 1 of Yamasaki shows communication module for an integrated circuit meant for delivering one output comprising means for generating main voltage (EX, not shown), means for generating an internal reference (RFG). The voltage of the reference voltage (Vref) is inherently lower than the supply voltage (EX) of the circuit; means for connecting the main voltage on the output (2d) and means (2b) for limiting the voltage on the output. The output voltage is equal to the reference voltage (col. 9. lines 18-23).

Regarding claims 22 and 23, figure 1 of Yamasaki shows communication module for an integrated circuit meant for delivering one output comprising means for generating main voltage (EX, not shown), means for generating an internal reference (RFG) an the voltage of the reference voltage (Vref) is inherently lower than the supply voltage (EX) of the circuit; means for connecting the main voltage on the output (2d) and means (2b) for limiting the voltage on the output. The output voltage is equal to the reference voltage (col. 9. lines 18-23). It is inherent that the reference voltage (vref) is used to supply other components of the integrated circuit (VDC). It is inherent that an input (gate) of a transistor of comparator (2b) is controlled by the reference voltage (Vref).

### ***Claim Rejections - 35 USC § 103***

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 13 and 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yamasaki (USP. 6,486,731).

Regarding claims 13 the recitations “ logic “1” of a USB connection” and is merely intended use thus, they do not further limit the limitations of the claims. It has been held that a recitation with respect to the manner in which a claimed apparatus is intended to be employed does not differentiate the claimed apparatus from a prior art apparatus satisfying the claimed

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structural limitations. Ex Parte Masham, 2 USPQ F.2d 1647 (1987). Therefore, these limitations have not been given patentable weight.

Regarding claim 15, figure 1 of Yamasaki includes all the limitations of claim 15 except for the limitation that the predetermined voltage has a value of 3V and the main voltage has a value of 5V. However, the particular values of the predetermined voltage and the main voltage recited by the Applicant are considered to be design expedient depending upon a particular environment or an application in which the circuit of Yamasaki is to be used. Lacking of showing any criticality, a skilled artisan would be motivated to select the predetermined voltage having a value of 3V and the main voltage having a value of 5V for conforming to the power requirement of the components of the integrated circuit. Thus, the limitation of having predetermined voltage with a value of 3V and the main voltage with a value of 5V will not be patentable under 35 U.S.C. 103(a).

#### ***Allowable Subject Matter***

Claims 7, 9, 10, 12 and 21 would be allowable if rewritten to overcome the rejection(s) under 35 U.S.C. 112, 2nd paragraph, set forth in this Office action and to include all of the limitations of the base claim and any intervening claims.

Claim 7 would be allowable because the prior art of records (USP 6,486, 731) fails to teach or suggest an integrated circuit in that the gate of the second transistor is connected to the gate of a third diode connected transistor.

Claims 9, 10 and 12 would be allowable because the prior art of records (USP 6,486, 731) fails to teach or suggest an integrated circuit comprises a blocking means having first and second current mirror as called for in claim 9.

Claim 21 would be allowable because the prior art of records (USP 6,486, 731) fails to teach or suggest an integrated circuit comprises a blocking means having first and second current mirrors connected to each other.

#### ***Conclusion***

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

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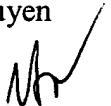
A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hiep Nguyen whose telephone number is (571) 272-1752. The examiner can normally be reached on Monday to Friday from 7:30am to 4:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy Callahan can be reached on (571) 272-1740. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Hiep Nguyen

10-05-05 TUAN T. LAM  
PRIMARY EXAMINER